

Publications

▪ Books

1. *Phase-Locked Loops: System Perspectives and Circuit Design Aspects*, W. Rhee and Z. Yu, Wiley-IEEE Press, Jan. 2024.
2. *Phase-Locked Frequency Generation and Clocking: Architectures and Circuits for Modern Wireless and Wireline Systems*, Edited by W. Rhee, The Institution of Engineering and Technology (IET), June 2020.
3. *Wireless Transceiver Circuits: System Perspectives and Design Aspects*, Edited by W. Rhee, CRC Press, Feb. 2015.

▪ Book Chapters

1. W. Rhee, "Evolution of monolithic phase-locked loops," in Chapter 1, *Phase-Locked Frequency Generation and Clocking: Architectures and Circuits for Modern Wireless and Wireline Systems*, Edited by W. Rhee, The Institution of Engineering and Technology (IET), pp. 3-29, June 2020.
2. N. Xu, W. Rhee, and Z. Wang, "FIR filtering techniques for clock and frequency generation," in Chapter 10, *Mixed Signal Circuits*, Edited by T. Noulis and M. Soma, CRC Press, pp. 261-278, Oct. 2015.
3. N. Xu, W. Rhee, and Z. Wang, "Hybrid phase modulators with enhanced linearity," in Chapter 17, *Wireless Transceiver Circuits: System Perspectives and Design Aspects*, Edited by W. Rhee, CRC Press, pp. 445-466, Feb. 2015.
4. X. Yu, W. Rhee, and Z. Wang, " $\Delta\Sigma$ phase-locked loops," in Chapter 12, *CMOS Nanoelectronics: Analog and RF VLSI Circuits*, Edited by K. Iniewski, McGraw Hill Publishers, pp. 411-436, Sept. 2011.
5. W. Rhee, "Practical design aspects in fractional- N frequency synthesis," *Analog Circuit Design*, Edited by A. van Roermund, M. Steyaert, and J. Huijsing, Kluwer Academic Publishers, pp. 3-26, 2003.
6. W. Rhee, B. Song, and A. Ali, "A 1.1-GHz CMOS fractional- N frequency synthesizer with a 3-b third-order delta-sigma modulator," *Phase-Locking in High Performance Systems: From Devices to Architectures*, Edited by B. Razavi, John Wiley & Sons, Inc., pp. 596-602, 2003.

▪ Articles

1. A. Altvater, "In Step With Woogeun Rhee: *Benefiting Humanity With Global Reach*," *IEEE Solid-State Circuits Magazine*, vol. 14, Issue 1, pp. 97-99, Jan. 2022.

▪ Journals

1. Y. Nie, W. Rhee, and Z. Wang, "An IEEE 802.15.4/z coherent quadrature hybrid correlation UWB receiver in 65-nm CMOS," accepted for *IEEE Journal of Solid-State Circuits*.
2. B. Zhou, Y. Li, Z. Wang, C. Wang, W. Rhee, and Z. Wang, "A low-complexity FM-UWB transmitter with digital reuse and analog stacking," accepted for *IEEE Journal of Solid-State Circuits*.
3. B. Wang, W. Rhee, and Z. Wang, "A 65-nm sub-10-mW communication/ranging quadrature uncertain-IF IR-UWB transceiver with twin-OOK modulation," accepted for *IEEE Journal of Solid-State Circuits*.
4. B. Wang, C. Ding, Y. Nie, W. Rhee, and Z. Wang, "A 0.14-nJ/b 200-Mb/s 2.7–3.5-GHz quasi-balanced FSK transceiver with PLL-based modulation and sideband energy detection," accepted for *IEEE Trans. Circuits and Systems I*, vol. 71, pp. 1590-1601, Apr. 2024.

5. L. Feng, W. Rhee, and Z. Wang, "A 2.6-GHz $\Delta\Sigma$ fractional-N BBPLL with FIR-embedded injection-locked-oscillator-based phase-domain lowpass filter," *IEEE Journal of Solid-State Circuits*, vol. 59, pp. 728-739, Mar. 2024.
6. S. Lee, B. Kang, W. Rhee, and D.-K. Jeong, "A 0.061-pJ/b/dB 28-Gb/s gradient-based maximum eye tracking CDR with 2-tap DFE adaptation in 28-nm CMOS," *IEEE Trans. Circuits and Systems II*, vol. 70, pp. 3998-4002, Nov. 2023.
7. L. Feng, W. Rhee, and Z. Wang, "A Quantization noise reduction method for delta-sigma fractional-N PLLs using cascaded injection-locked oscillators," *IEEE Trans. Circuits and Systems II*, vol. 69, pp. 2448-2452, May 2022.
8. M. Ni, X. Wang, F. Li, W. Rhee, and Z. Wang, "A 13-Bit 2-GS/s time-interleaved ADC with improved correlation-based timing skew calibration strategy," *IEEE Trans. Circuits and Systems I*, vol. 69, pp. 481-494, Feb., 2022
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12. C. Ding, B. Wang, H. Song, W. Rhee, and Z. Wang, "A 3.5-GHz 0.24-nJ/b 100-Mb/s fully balanced FSK receiver with sideband energy detection," *IEEE Solid-State Circuits Letters*, vol. 4, 2021.
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14. H. Song, D. Liu, Y. Zhang, W. Rhee, and Z. Wang, "A 6.5–8.1-GHz communication/ranging VWB transceiver for secure wireless connectivity with enhanced bandwidth efficiency and $\Delta\Sigma$ energy detection," *IEEE Journal of Solid-State Circuits*, vol. 55, pp. 219-232, Feb. 2020.
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- Invited Talks in International Conferences & Workshops
1. W. Rhee, RFIC, Jan. 2024
 2. W. Rhee, "PLL architectures, tradeoffs, and key application considerations," *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, Feb. 2021. (online)
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 6. W. Rhee, "Phase-locked frequency synthesis and modulation," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, May 2018.
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 8. W. Rhee, "Phase-locked clock generation for SoC: Circuit and system design aspects," *IEEE NEWCAS*, Vancouver, Canada, June 2016.
 9. W. Rhee, "Ultra-wideband technology for short-range communications," *CMOS Emerging Technologies*, Vancouver, Canada, June, 2016.
 10. W. Rhee, "Phase-locked frequency synthesis and modulation for modern wireless transceivers," *IEEE Custom Integrated Circuits Conference (CICC)*, San Jose, CA, USA, September 2015.
 11. W. Rhee, "Phase-locked clock generation for SoC: Circuit and system design aspects," *IEEE International System-on-Chip Conference (SOCC)*, Beijing, China, September 2015.
 12. W. Rhee, "Phase-locked clocking and frequency synthesis - System perspectives tailored for IC designers," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Lisbon, Portugal, May 2015.
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